Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **OUTPUT A**
2. **– INPUT A**
3. **+ INPUT A**
4. **GND**
5. **+ INPUT B**
6. **– INPUT B**
7. **OUTPUT B**
8. **V +**

**.052”**

**MASK**

**REF**

**1 8 7**

**3 4 5**

**2**

**6**

**.042”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GROUND**

**Mask Ref: C**

**APPROVED BY: DK DIE SIZE .042” X .052” DATE: 11/11/21**

**MFG: NATIONAL THICKNESS .015” P/N: LM358A**

**DG 10.1.2**

#### Rev B, 7/19/02